CLAIMS

What is claimed is:

1. An electrical circuit for generating a differential data signal and a squelch state over a differential signal pair, the differential signal pair having a positive signal line and a negative signal line, the circuit comprising:

a current-mode logic (CML) buffer having a true data input, a true data output and a complementary data output, the true data output driving the positive signal line, the complementary data output driving the negative signal line, the data input being driven by a data input signal; and

a CML multiplexer having a first and second true data inputs, an input selector, a true data output and a complementary data output, the first true data input being driven by the data input signal, the second true data input being driven by a logical inversion of the data input signal, the input selector being driven by a squelch state signal, the true data output being coupled with the true data output of the CML buffer, and the complementary data output being coupled with the complementary data output of the CML buffer.

2. The electrical circuit of claim 1, wherein the CML buffer also has a complementary data input driven by the logical inversion of the data input signal.

3. The electrical circuit of claim 1, wherein the CML multiplexer also has a first and a second complementary data input, the first complementary data input being driven by the logical inversion of the data input signal, the second complementary data input being driven by the data input signal.

4. The electrical circuit of claim 1, wherein the CML buffer and the CML multiplexer are discrete electronic components.

5. The electrical circuit of claim 1, wherein the CML buffer and the CML multiplexer are logic circuits implemented within a single integrated circuit.

6. The electrical circuit of claim 1, wherein the CML buffer and the CML multiplexer each have back-termination impedances approximately twice the value of the characteristic impedance of the positive signal line and the negative signal line.

7. The electrical circuit of claim 1, further comprising:

a first series resistor connected to the true data output of the CML buffer; and

a second series resistor connected to the complementary data output of the CML buffer, the second series resistor being of substantially equal value to that of the first series resistor, the values of the first and second series resistors being such that the difference between the voltages of the positive signal line and the negative signal line remain within a predetermined limit when the squelch state signal is active.

8. The electrical circuit of claim 7, wherein the first and second series resistors are on-chip resistors.

9. The electrical circuit of claim 7, wherein the first and second series resistors are external fixed resistors.

10. The electrical circuit of claim 7, wherein the first and second series resistors are potentiometers.

11. The electrical circuit of claim 1, further comprising:

a first series resistor connected to the true data output of the CML multiplexer; and

a second series resistor connected to the complementary data output of the CML multiplexer, the second series resistor being of substantially equal value to that of the first series resistor, the values of the first and second series resistors being such that the difference between the voltages of the positive signal line and the negative signal line remain within a predetermined limit when the squelch state signal is active.

12. The electrical circuit of claim 11, wherein the first and second series resistors are on-chip resistors.

13. The electrical circuit of claim 11, wherein the first and second series resistors are external fixed resistors.

14. The electrical circuit of claim 11, wherein the first and second series resistors are potentiometers.